

# VINAY C JAVALI

Electronics and Communication Enginner

✉ [vinay.javali@outlook.com](mailto:vinay.javali@outlook.com) ☎ 6361304263 📍 Hubballi 🌐 <https://www.linkedin.com/in/vinaycjavali>

## Summary

Electronics and Communication Engineering student with knowledge of semiconductor technology, electronic circuits, and communication systems. Strong analytical and problem-solving abilities, complemented by hands-on project experience and a commitment to continuous learning , professional growth and looking forward to contribute to the organization.

## Education

|                                                                              |                                     |
|------------------------------------------------------------------------------|-------------------------------------|
| <b>KLE Technological University</b><br>Electronics and Communication         | Bachelor of Engineering<br>Hubballi |
| <b>Tippu Shaheed Institute of Technology</b><br>Electronics and communicatin | Diploma<br>Hubballi                 |

## Experience

|                                                                    |                                 |
|--------------------------------------------------------------------|---------------------------------|
| <b>YQ14 Technologies Pvt.Ltd.</b><br>Intern Analog layout Enginner | Bangalore<br>Jan 2026 – Present |
|--------------------------------------------------------------------|---------------------------------|

## Projects

### Voltage Regulator Layout Design in 40nm Technology

- Designed and implemented the analog layout of a Voltage Regulator in 40nm technology using Cadence Virtuoso. Performed device matching, floorplanning, routing, and DRC/LVS verification while optimizing the layout for stability, area, and performance.

### CMOS Operational Amplifier Layout Design

- Implemented a 40nm CMOS Operational Amplifier layout using Cadence Virtuoso, applying industry-standard layout practices such as common-centroid matching, routing optimization, and parasitic minimization. Verified design correctness through DRC and LVS checks

### System-Level Simulation and Performance Evaluation of 5G NR Network using Matlab

- Developed a MATLAB-based 5G NR network simulator to evaluate SINR, throughput, and interference in multi-cell environments. Implemented 3GPP UMa channel modeling and analyzed network performance under various user deployment scenarios.

### Testing of 5G Private Network using OAI

- successfully built the 5G private network and tested the network and gone through some changes in the network. where there is no interruptions in the network.

### A DeepFake Detection Study

- Developed a DeepFake image detection system using a custom CNN to classify real and fake images. Implemented image preprocessing and data augmentation using Python, TensorFlow, and Keras. Compared multiple deep learning models and achieved 90.44% testing accuracy.

## Technical Skills

### Programming Language

C programming, C++, Phyton

### Analog Layout

Analog Layout Design, CMOS Technology (40nm), Device Matching, Floorplanning, DRC & LVS Concepts, CMOS Layout Techniques

### EDA Tools & Software

Cadence Virtuoso, Calibre, Assura, LTspice

---

**Verification & Validation**

DRC (Design Rule Check), LVS (Layout Versus Schematic), ERC (Electrical Rule Check)

**Technology & Fundamentals**

Semiconductor Fundamentals, Analog IC Design Basics, CMOS Technology (40nm), VLSI Design Flow, MOSFET Characteristics

---

**Certification**

**Juniper network - Junos, Associate (JNCIA-Junos)**

**Full Stack Embedded Systems - Krutanic**

---

**Awards**

SAE BAJA - 2025  
M-BAJA - AIR 5th  
  
SAE BAJA - 2024  
M-BAJA - AIR 9th

---

**Member**

**KLE TECH Motorsports (Member)**  
Hubballi

2023 – 2025

---

**Soft Skills**

**skills**  
Critical Thinking, Attention to Detail, Communication, Time Management, Problem Solving, Adaptability